UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,461	05/08/2001	Toru Aida	FURUSAWA 57	4329

7590 11/26/2004

Flynn Thiel Boutell & Tanis
2026 Rambling Road
Kalamazoo, MI 49008-1699

EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,461	AIDA ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☒ Claim(s) 2-7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: in claim 1, "coefficient memory for predetermined filter coefficients corresponding to plurality of magnifications" should instead read "coefficient memory for ***storing*** or ***memorizing*** predetermined filter coefficients corresponding to plurality of magnifications". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim **1** is rejected under 35 U.S.C. 102(e) as being anticipated by Kang, U.S. Pat. No. 6,404,458.

Considering claim **1**, Kang discloses all claimed subject matter, note;

a) an image memory for storing the inputted image data, is met by Line Memory Unit 205, fig.3;

b) coefficient memory for predetermined filter coefficients corresponding to plurality of magnifications, **is inherent** in Kang because the coefficients that are generated (see Fig.6) and controlled by coefficient controller 204-1 must be stored in a memory or storage device.

c) non-linear magnification controller for not only outputting the enable signal to read out the corresponding image data from the image memory according to any given magnification set for the n number of areas and area width w provided by dividing image to be displayed into n number any larger integer) of equal areas but also for outputting the coefficient selection address to read out the corresponding filter coefficient from the coefficient memory, is met by the coefficient controller 204-1, fig.3;

d) a filter for filtering the image data read out from the image memory according the filtering coefficient read out from the coefficient memory but also outputting the image data processed for enlargement according to any magnification set for each of the n number of areas arranged in horizontally, is met by Sample interpolation unit, fig. 3;

Allowable Subject Matter

4. Claims **2-7** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose an image magnifying circuit wherein the coefficient memory comprises a coefficient ROM (Read Only Memory) for storing the predetermined filter coefficients corresponding to a plurality of magnifications, a memory controller for not only reading out the filter coefficient from the coefficient ROM according to a transfer start signal but also for outputting the coefficient writing address and R/W selection signal, a selector for selecting either one of the coefficient selection address outputted from the non-linear magnification controller or the coefficient writing address outputted from the memory controller according to the R/W (Read/Write) selection signal outputted from the memory controller, and a coefficient RAM (Random Access Memory) for not only storing the filter coefficient read out from the coefficient ROM according to the coefficient writing address outputted from the selector when an image magnifying circuit, as in claim 2;

Wherein the non-linear magnification controller comprises an area selection signal generator for generating the area selection signal for sequentially selecting the n number (n any larger integer) areas according to the set area width a first selector for selecting, for output, the magnification parameter m (m a positive number 2n or less; 2n represents the second power of 2; magnification is equivalent to 2n/m) set for the corresponding area according to the area selection signal generated by the area selection signal generator, an n-bit adder for receiving, as one of the inputs, the magnification parameter m selected by the first selector, an address offset arithmetic-logic unit for calculating the start point of the coefficient selection address according to

the input of the magnification parameter m set for the selection start area of the n number of areas, second selector for selecting, for output, the calculated value of the address offset arithmetic-logic unit and the sum-data the adder, first delayer for delaying the output value the second selector by 1 sampling period for output not only as a coefficient selection address but also another input to the adder, logical sum circuit for outputting the logical sum signal of the carry signal the adder and the initializing signal, and a second delayer for delaying the output signal the logical sum circuit by 1 sampling period for output as an enable signal the image memory, as in claim 3;

The image magnifying circuit, wherein the area selection signal generator comprises a dot counter for counting the dot clock, the dot counter being provided with a load terminal L1 for loading the initial signal as a counted value 1, a coincidence detection circuit for not only comparing the counted value of the dot counter with the set area width w or 2 times the set area width w to detect that they are coincidence with each other but also for outputting the detection signal, as a counted value 1, to the load terminal L1 of the dot counter, an up/down counter, which can be reset by the initializing signal, for not only counting the dot clock according to the enable signal, which is the detection signal of the coincidence circuit, but also for outputting the counted value as the area selection signal, an up/down controller for not only controlling the up/down counter to the up-count mode by outputting the H-level signal when the counted value of the up/down counter has become 0 but also for controlling the up/down counter to the down-count mode according to the detection signal of the coincidence detection circuit after the counted value K of the up/down counter has varied to the value corresponding

to the central areas of the image to be displayed, and a area width controller for not only for outputting the set area width w, as a comparison value,' to the coincidence detection circuit in the initial state but also for outputting 2 times the set area width w, as a comparison value, to the coincidence detection circuit when the counted value K of the up/down counter has varied to the value corresponding to the central areas of the image to be displayed, as in claim 4.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. **Kang,** U.S. Pat. No. **6,191,820** discloses device and method for converting aspect ratio of video signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
November 23, 2004

PAULOS M. NATNAEL
PATENT EXAMINER